11-12-03

AF

Express Mail Label No. EV411109150US

PATENT APPLICATION
Docket No.: 11675.107

OIPE JC16 NOV 10 2003 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of		)
	David Y. Kao Fernando Gonzalez	)
Serial No.:	08/720,693	) Art Unit
Filed:	October 2, 1996	) 2823
For:	OXIDATION OF ION IMPLANTED SEMICONDUCTORS	)
Confirmation No.:	1934	)
Examiner:	George R. Fourson III	)

TRANSMITTAL OF APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is a Brief of Appellants for entry in the above-identified application. Appellants have filed a timely Notice of Appeal from the action of the Examiner dated May 9, 2003. Also enclosed are the following:

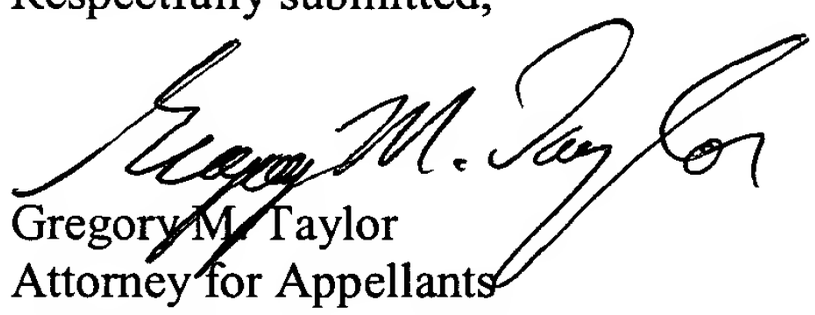
x A Certificate of Express Mail Under 37 C.F.R. § 1.10

x Credit Card Payment Form PTO-2038 authorizing payment of $330.00 for the filing fee.

x The Commissioner is hereby authorized to charge payment of any patent application processing fees under 37 CFR 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-3178. Duplicate copies of this sheet are attached.

Dated this 10th day of November 2003.

Respectfully submitted,

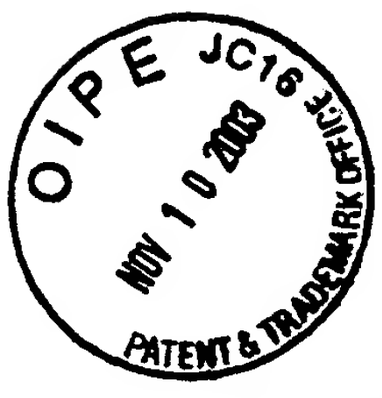


Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\107\VFW0000002658V001.doc

Express Mail Label No. EV411109150US

PATENT APPLICATION
Docket No.: 11675.107



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of		)
	David Y. Kao Fernando Gonzalez	)
Serial No.:	08/720,693	) Art Unit
Filed:	October 2, 1996	) 2823
For:	OXIDATION OF ION IMPLANTED SEMICONDUCTORS	)
Confirmation No.:	1934	)
Examiner:	George R. Fourson III	)

CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10

I hereby certify that the following documents are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 10th day of November 2003.

- Brief of Appellant
- Credit Card Payment Form PTO-2038 for $330.00
- Transmittal Letter
- Postcard

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\107\VFW0000002658V001.doc

OIPE
NOV 10 2003
PATENT & TRADEMARK OFFICE

Express Mail Label No. EV411109150US

PATENT APPLICATION
Docket No.: 11675.107

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of		)
	David Y. Kao Fernando Gonzalez	)
Serial No.:	08/720,693	) Art Unit
Filed:	October 2, 1996	) 2823
For:	OXIDATION OF ION IMPLANTED SEMICONDUCTORS	)
Confirmation No.:	1934	)
Examiner:	George R. Fourson III	)

BRIEF OF APPELLANTS

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants, David Y. Kao and Fernando Gonzalez, have filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims in this application. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $330.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

11/14/2003 AWONDAF1 00000080 08720693
01 FC:1402 330.00 OP

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from David Y. Kao and Fernando Gonzalez, who are the named inventors and are captioned in the present brief. The assignment documents were recorded at Reel No. 8192, Frame 0741 in the United States Patent and Trademark Office on October 2, 1996.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 2-4, 7-19, 22-33, and 45-49 are pending and appealed in the present application.

Claims 1, 5-6, 20-21, and 34-44 have been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention is a method for forming an oxide region on a substrate assembly. The method comprises providing a substrate assembly 12 having a first semiconductor material and a masking substrate 20 thereover (Figs. 2 and 9). The masking substrate comprises at least one unmasked opening 20a that has an opening width, such that the unmasked opening is defined by a masking substrate-free region on the substrate assembly. Spacers 40 are formed in the masking substrate, with the unmasked opening being defined by the spacers, and each of the spacers extend from the substrate assembly to contact the masking substrate (Fig. 9). Ions are

selected to be implanted into the first semiconductor material as implantation ions, wherein the selecting is performed such that the ions do not alter the electrical charge characteristics of the first semiconductor material, and such that the masking substrate is impermeable to the ions. The implantation ions 34 are bombarded through the unmasked opening 20a on the first semiconductor material to produce an implanted region (Fig. 9). An oxide 42 of the first semiconductor material is formed throughout the opening width by exposing the implanted region to a gas phase oxidant (Fig. 10). No additional layer is formed within the unmasked opening after the bombarding and prior to forming the oxide.

ISSUES

1. Whether claims 7-11, 13-19, 22-33, and 45-49 are unobvious over U.S. Patent No. 5,869,385 to Tang et al. (hereafter "*Tang*") in combination with the article by Minegishi et al. (hereafter "*Minegishi*").

2. Whether claims 2-4 are unobvious over *Tang* in combination with *Minegishi* and further in view of Japanese Patent No. 5-175190 (hereafter JP '190).

3. Whether claim 12 is unobvious over *Tang* in combination with *Minegishi* and further in view of Japanese Patent No. 62-48028 (hereafter JP '028).

GROUPING OF CLAIMS

Claims 2-4, 7-11, 12, 13-19, 22-33, and 45-49 stand or fall together.

ARGUMENT

1. Claims 7-11, 13-19, 22-33, and 45-49 are Unobvious Over *Tang* in Combination with *Minegishi*

Claims 7-11, 13-19, 22-33, and 45-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tang* in combination with *Minegishi*. For the reasons that follow, Appellants respectfully submit that claims 7-11, 13-19, 22-33, and 45-49 are unobvious over *Tang* in combination with *Minegishi*.

The law is well settled that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122, 8th ed. (Aug. 2001).

Independent claim 47 in the present application recites forming spacers in the masking substrate. There is no teaching or suggestion in *Tang* of formation of spacers in the patterned layer disclosed therein. While *Minegishi* teaches formation of a spacer (frame) in a selective oxidation process, there is no teaching or suggestion that such a spacer would be suitable for use in the process disclosed in *Tang*. It is an improper hindsight reconstruction to combine elements from two different prior art references to achieve the claimed invention without any motivation for doing so other than Appellants' disclosure.

Independent claims 32 and 49 in the present application recite that silicon ions are implanted into the substrate. In contrast, *Minegishi* only discloses that boron ions are implanted

for channel stopper after the framed mask fabrication step (page 56, col. 1). It is well know that boron ions are electrically conducting, whereas silicon ions are non-electrically conducting (*see Tang*, col. 6, lines 58-62). Further, claim 47 recites that the ions do not alter the electrical charge characteristics of the semiconductor material. Thus, there is no suggestion that the process of *Minegishi*, which uses boron ion implantation with a spacer, would be suitable in a method that uses silicon ion implantation or implantation of ions that do not alter the electrical charge characteristics of the semiconductor material.

Accordingly, claims 7-11, 13-19, 22-33, and 45-49 would not have been obvious over *Tang* in combination with *Minegishi*. Appellants therefore respectfully request that the rejection of claims 7-11, 13-19, 22-33, and 45-49 under 35 U.S.C. § 103(a) be overturned.

2. Claims 2-4 are Unobvious over *Tang* in Combination with *Minegishi* and Further in View of JP '190

Claims 2-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tang* in combination with *Minegishi* and further in view of JP '190. For the reasons that follow, Appellants respectfully submit that claims 2-4 are unobvious over *Tang* in combination with *Minegishi* and further in view of JP '190.

Claims 2-4 depend from claim 47 and thus include the limitations thereof. As discussed above with respect to claim 47, there is no teaching or suggestion in *Tang* of formation of spacers in the pattered layer disclosed therein, and there is no motivation to combine the teachings of *Minegishi* and *Tang*. In addition, there is no teaching or suggestion in JP '190 of the formation of spacers in the patterned film disclosed therein.

Accordingly, claims 2-4 would not have been obvious over *Tang* in combination with *Minegishi* and further in view of JP '190. Appellants therefore respectfully request that the rejection of claims 2-4 under 35 U.S.C. § 103(a) be overturned.

3. Claim 12 is Unobvious over *Tang* in Combination with *Minegishi* and Further in View of JP '028

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tang* in combination with *Minegishi* and further in view of JP '028. For the reasons that follow, Appellants respectfully submit that claim 12 is unobvious over *Tang* in combination with *Minegishi* and further in view of JP '028.

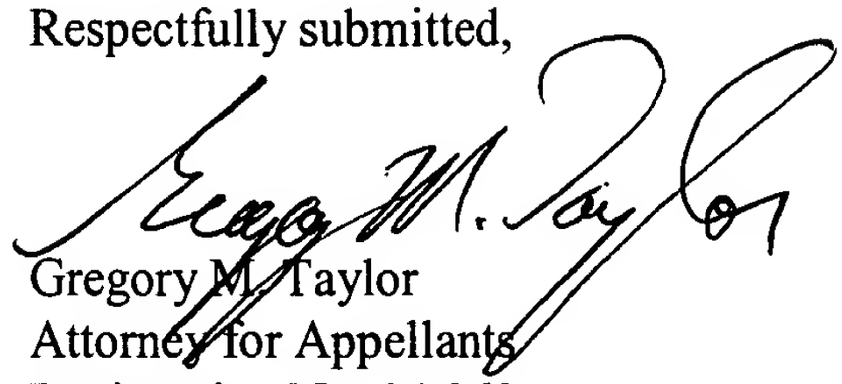
Claim 12 depends indirectly from claim 47 and thus includes the limitations thereof. As discussed above with respect to claim 47, there is no teaching or suggestion in *Tang* of formation of spacers in the pattered layer disclosed therein, and there is no motivation to combine the teachings of *Minegishi* and *Tang*. In addition, there is no teaching or suggestion in JP '028 of the formation of spacers.

Accordingly, claim 12 would not have been obvious over *Tang* in combination with *Minegishi* and further in view of JP '028. Appellants therefore respectfully request that the rejection of claim 12 under 35 U.S.C. § 103(a) be overturned.

In view of the foregoing, Appellants respectfully request the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 10th day of November 2003.

Respectfully submitted,



Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\107\VFW0000002650V001.doc

APPENDIX: CLAIMS ON APPEAL

2. A method as recited in Claim 47, wherein said implantation ions comprise ions of said first material and ions that are different from said ions of said first material.

3. A method as recited in Claim 2, wherein the implantation ions of said first material comprise silicon ions.

4. A method as recited in Claim 3, wherein said first material comprises monocrystalline silicon.

7. A method as recited in Claim 47, wherein said forming spacers further comprises:

depositing a layer of spacer material over the opening in the masking substrate; and

etching the layer of spacer material to form the spacers around the opening.

8. A method as recited in Claim 7, wherein the layer of spacer material comprises silicon nitride.

9. A method as recited in Claim 7, wherein said etching the layer of spacer material is an anisotropic etch.

10. A method as recited in Claim 9, wherein said opening width is in the range from about 0.05 micrometers to about 0.1 micrometers.

11. A method as recited in Claim 47, further comprising the steps, prior to said bombarding through said unmasked opening of:

forming a pad oxide layer on said first semiconductor material;

forming a masking substrate comprising a nitride layer over the pad oxide layer;

forming a photoresist mask over the nitride layer; and

selectively removing the nitride layer through the photoresist mask to expose through said unmasked opening said first semiconductor material, wherein the first semiconductor material is oxidized in the region within said unmasked opening.

12. A method as recited in Claim 11, wherein the photoresist mask is removed after said bombarding through said unmasked opening of said first semiconductor material with implantation ions of said first material.

13. A method as recited in Claim 11, wherein said selectively removing the nitride layer through the photoresist mask includes selectively removing the nitride layer and selectively removing the pad oxide layer.

14. A method as recited in Claim 47, wherein said first semiconductor material has a top surface, and wherein said implantation ions are directed towards said first semiconductor material in a direction that is within ten degrees from a direction that is orthogonal to the top surface.

15. A method as recited in Claim 47, wherein said forming an oxide further comprises heating said substrate assembly while exposing the substrate assembly to oxygen.

16. A method as recited in Claim 47, wherein said first semiconductor material comprises a monocrystalline material having a lattice structure, wherein the implantation ions cause the lattice structure of the monocrystalline material to become partially randomized at the region into which said ions are implanted.

17. A method as recited in Claim 16, wherein both the monocrystalline material and said implantation ions comprise silicon.

18. A method as recited in Claim 47, wherein said exposing said implanted region is conducted at a pressure in the range from about 1 atmosphere to about 25 atmospheres.

19. A method as recited in Claim 47, wherein said exposing said implanted region is conducted at a pressure in the range from about 5 atmospheres to about 25 atmospheres.

22. A method as recited in Claim 49, wherein said forming a spacer around the opening in the hard mask comprises:

depositing a layer of spacer material over the opening in the hard mask; and

anisotropically etching the layer of spacer material at the opening in the hard mask to form the spacer situated around the opening of the hard mask.

23. A method as recited in Claim 49, wherein the spacer around the opening in the hard mask comprises silicon nitride.

24. A method as recited in Claim 49, wherein the spacer is one of a pair of spacers, the ions being implanted in between but not through the pair of spacers and past the hard mask into the exposed region of the volume of silicon, and wherein the exposed region is situated between the pair of spacers, whereby the silicon dioxide is not substantially formed underneath the pair of spacers.

25. A method as recited in Claim 24, wherein the pair of spacers are separated by a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

26. A method as recited in Claim 49, further comprising forming a pad oxide layer upon the volume of silicon prior to forming the hard mask over the volume of silicon of the substrate assembly, the hard mask being formed upon the pad oxide layer, and said forming a hard mask over a volume of silicon of a substrate assembly comprising:

forming the hard mask upon the pad oxide layer; and

forming a photoresist mask over the hard mask; and wherein silicon dioxide is formed in the volume of silicon at the region beneath the opening in the hard mask.

27. A method as recited in Claim 26, wherein the photoresist mask is removed after said bombarding the exposed region of the volume of silicon.

28. A method as recited in Claim 26, wherein said forming an opening in the hard mask comprises etching through the hard mask upon the pad oxide layer.

29. A method as recited in Claim 49, wherein the exposed region of a volume of silicon has a top surface, and said bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask is conducted such that the direction that the ions are implanted into the exposed region is within ten degrees from a direction that is orthogonal to the top surface.

30. A method as recited in Claim 49, wherein said oxidizing the volume of silicon to form silicon dioxide further comprises heating the substrate assembly while exposing the substrate assembly to oxygen.

31. A method as recited in Claim 49, wherein the volume of silicon comprises monocrystalline silicon having a lattice structure, and wherein the implanted silicon ions in the monocrystalline silicon cause the lattice structure of the monocrystalline silicon to become partially randomized at the exposed region into which the ions are implanted.

32. A method for forming an oxide region on a substrate assembly, the method comprising the steps of:

forming a hard mask over a pad oxide layer situated on a volume of silicon of a substrate assembly, the substrate assembly having a top surface;

forming an opening in the hard mask to expose a region of the volume of silicon, said region of said volume of silicon comprising monocrystalline silicon having a lattice structure;

depositing a layer of silicon nitride over the opening of the hard mask;

etching the layer of silicon nitride and the pad oxide layer to form a pair of silicon nitride spacers situated on opposite sides of the opening of the hard mask and having said exposed region of the volume of silicon therebetween, each said silicon nitride spacer extending from the volume of silicon to contact the hard mask; and

forming silicon dioxide in the region between said pair of spacers by kinetically regulating silicon oxidation, wherein said kinetically regulating silicon oxidation comprises:

implanting silicon ions between but not through the pair of silicon nitride spacers and through the opening in the hard mask into the exposed region of the volume of silicon such that the direction that the silicon ions are implanted into the exposed region is within ten degrees of a direction that is orthogonal to the top surface of the substrate assembly, wherein the implanted silicon ions do not substantially alter the conductivity type of the region, and wherein the implanted silicon ions in the monocrystalline silicon in the exposed region cause the lattice structure thereof to become partially randomized; and

heating the substrate assembly and exposing the substrate assembly to oxygen so as to form silicon dioxide at the exposed region, whereby the silicon layer oxidizes faster where the silicon ions are implanted than where the silicon ions are not implanted, wherein said silicon dioxide has substantially uniform thickness throughout said exposed region, wherein said kinetically regulating silicon oxidation is performed through said opening having a width that is substantially the same at said implanting as it is at said heating and said exposing, and wherein no additional layer is formed within said opening during said kinetically regulating silicon oxidation.

33. A method as recited in Claim 32, wherein the pair of spacers are separated by a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

45. A method as recited in Claim 47, wherein said implantation ions are different from ions of said first semiconductor material.

46. A method as recited in Claim 47, further comprising bombarding through said unmasked region with implantation ions that are different from ions of said first semiconductor material.

47. A method for forming an oxide region on a substrate assembly, the method comprising:

providing a substrate assembly having a first semiconductor material and a masking substrate thereover, wherein said masking substrate comprises at least one unmasked opening that has an opening width, such that said unmasked opening is defined by a masking substrate-free region on said substrate assembly, wherein said masking substrate-free region has a width that is said opening width;

forming spacers in said masking substrate, wherein said unmasked opening is defined by said spacers, and each of said spacers extends from the substrate assembly to contact said masking substrate;

selecting ions to be implanted into said first semiconductor material as implantation ions, wherein said selecting is performed such that said ions do not alter the electrical charge characteristics of said first semiconductor material, and such that said masking substrate is impermeable to said ions;

bombarding through said unmasked opening said first semiconductor material with implantation ions to produce an implanted region; and

forming an oxide of said first semiconductor material throughout said opening width by exposing said implanted region to a gas phase oxidant, wherein said bombarding and said exposing are performed through said unmasked opening, and said bombarding and said exposing are performed over the entire opening width of said unmasked opening, and no additional layer is formed within said unmasked opening after said bombarding and prior to said forming an oxide.

48. A method as recited in Claim 47, wherein said implantation ions are ions of said first semiconductor material.

49. A method for forming an oxide region on a substrate assembly, the method comprising:

forming a hard mask over a volume of silicon of a substrate assembly;

forming an opening in the hard mask to expose a region of the volume of silicon;

forming a spacer around the opening in the hard mask, said spacer extending from the volume of silicon to contact the hard mask;

bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask so as to leave unaltered the conductivity type of the exposed region of the volume of silicon, wherein said bombarding implants silicon ions immediately adjacent to but not through the spacer around the opening in the hard mask; and

oxidizing the volume of silicon to form silicon dioxide by exposure through said opening of the exposed region to oxygen, wherein said bombarding and said oxidizing are performed through said opening having a width that is substantially the same at said bombarding as at said oxidizing, and wherein no additional layer is formed within said opening after said bombarding and prior to said oxidizing.